Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

1. (cancelled)

2. (currently amended) The method of Claim ~~1~~ 23, further comprising decoding the plurality of instructions within a single clock cycle.

3. (cancelled)

4. (currently amended) The method of Claim ~~1~~ 23, further comprising decoding width bits to determine the size of the instructions.

5. (currently amended) The method of Claim ~~1~~ 23, where a number of simultaneous instructions is greater than 1, and further comprising communicating the number and size of the plurality of instructions to the decoder.

6. (currently amended) The method of Claim ~~1~~ 23, further comprising loading a first of the plurality of instructions having a first size and a second of the plurality of instructions having a second size different than said first size.

7. (original) The method of Claim 6, further comprising loading a first of the plurality of instructions having a first size, and loading a second and a third of the plurality of instructions having a second size, wherein the first size is 32-bits and the second size is 16-bits.

8. (currently amended) The method of Claim ~~1~~ 23, handling the plurality of instructions within a digital signal processor.

9. (currently amended) A method of decoding a plurality of instructions within a processor comprising:

determining ~~the~~ a size of the plurality of instructions;

loading the plurality of instructions simultaneously into an instruction register, said plurality of instructions including two or more instructions received from different ones of a plurality of instruction sources, where the plurality of

instruction sources are each associated with a different location in an instruction pipeline;

presenting the plurality of instructions from ~~an~~ the instruction register to a decoder; and

decoding ~~each~~ all of the plurality of instructions within a single clock cycle.

10. (original) The method of Claim 7, further comprising simultaneously presenting each of the plurality of instructions to the decoder.

11. (original) The method of Claim 7, further comprising pre-decoding the plurality of instructions to determine the width of the plurality of instructions.

12. (original) The method of Claim 7, further comprising loading a next plurality of instructions into the single instruction register.

13. (original) The method of Claim 9, further comprising decoding a plurality of instructions in a digital signal processor.

14. (currently amended) A processor comprising:

an instruction register capable of holding a plurality of instructions, said plurality of instructions including two or more instructions received from different ones of a plurality of instruction sources, where the plurality of instruction sources are each associated with a different location in an instruction pipeline;

one or more pre-decoders which determines the size and number of the plurality of instructions; and

a decoder which substantially simultaneously receives the plurality of instructions from the instruction register, and the size and number from said at least one pre-decoder wherein the decoder decodes each of the plurality of instructions within a single clock cycle.

15. (original) The processor of Claim 14, wherein the pre-decoder determines width bits.

16. (canceled)

17. (original) The processor of Claim 14, wherein the pre-decoder communicates the number and size of the plurality of instructions to the decoder.

18. (original) The processor of Claim 14, wherein the processor is a digital signal processor.

19-22. (cancelled)

Please add the following new claims:

23. (new) A method, comprising:

receiving instructions and size information associated with the instructions from a plurality of different instruction sources, into a switching part, each instruction source associated with a different location in an instruction pipeline; and

using the switching part to switch among the instruction sources, said using providing an instruction and associated size information at an output thereof;

receiving the output from the switching part into a decoder; and

using the decoder to decode each instruction, using said associated size information.

24. (new) A method as in claim 23, wherein said receiving instructions comprises receiving a plurality of instruction simultaneously and size associated with said plurality of instructions, and decoding the plurality of instructions substantially simultaneously.

25. (new) An apparatus comprising:

a plurality of instruction sources, each associated with a different location in an instruction pipeline;

an instruction size determination unit, producing instruction sizes respectively associated with said plurality of instruction sources;

first and second switching elements, which respectively switch instructions from said instruction sources, and sizes from said instruction size determination unit, so that both said instructions and said instruction sizes are simultaneously output; and

a decoder, which receives said instructions and instruction sizes as inputs thereof.

26. (new) An apparatus as in claim 25, wherein said first and second switching elements switch multiple instructions to the decoder at the same time said determination unit also

providing an indication of a number of instructions, and said decoder simultaneously decodes said multiple instructions